IHP

SG13G2

open source

Process Specification

Rev. 1.2 (2023_12_20)

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1 General Information

SG13S is a high performance BiCMOS technology with a 0.13 µm CMOS process. It contains bipolar devices based on SiGe:C npn-HBT's with up to 250 GHz transit frequency (f_T) and 300 GHz maximum oscillation frequency. This process provides 2 gate oxides: A thin gate oxide for the 1.2 V digital logic and a thick oxide for a 3.3 V supply voltage. For both modules NMOS, PMOS and isolated NMOS transistors are offered. Further passive components like poly silicon resistors and MIM capacitors are available. The backend option offers 5 thin Al metal layers, two thick Al metal layers (2 and 3 µm thick)and a MIM layer.

SG13G2 has the same device portfolio as SG13S but much higher bipolar performance with f_T = 300 GHz and 500 GHz maximum oscillation frequency.

1.1 Main Processing Sequence and Cross-Section Schematic

- Shallow trench isolation (STI)
- NWell formation
- PWell formation
- Triple Well formation
- Poly Gate formation
- Bipolar Window opening
- Collector Window opening
- Emitter opening
- Emitter Poly definition
- Base Poly definition
- nSD implant / drive
- pSD implant / drive
- Salicide formation
- Contact definition
- Metal1
- Via1
- Metal2
- Via2
- Metal3
- Via3
- Metal4
- Via4
- Metal5
- MIM formation
- TopVia1
- TopMetal1
- TopVia2
- TopMetal2
- Passivation
- Parametric test

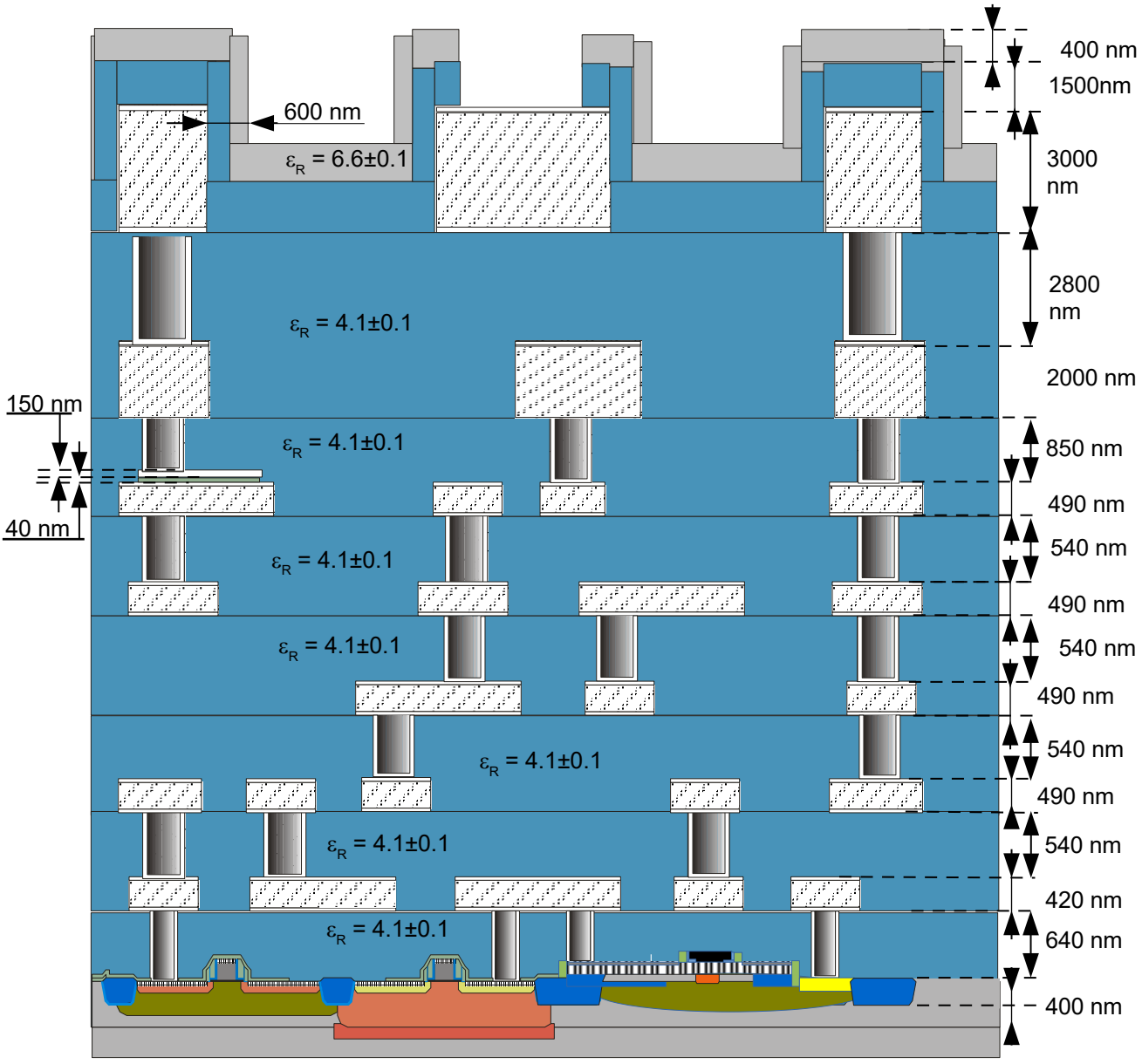


***Fig. 1.1.1: SG13** process cross-section (not to scale)*

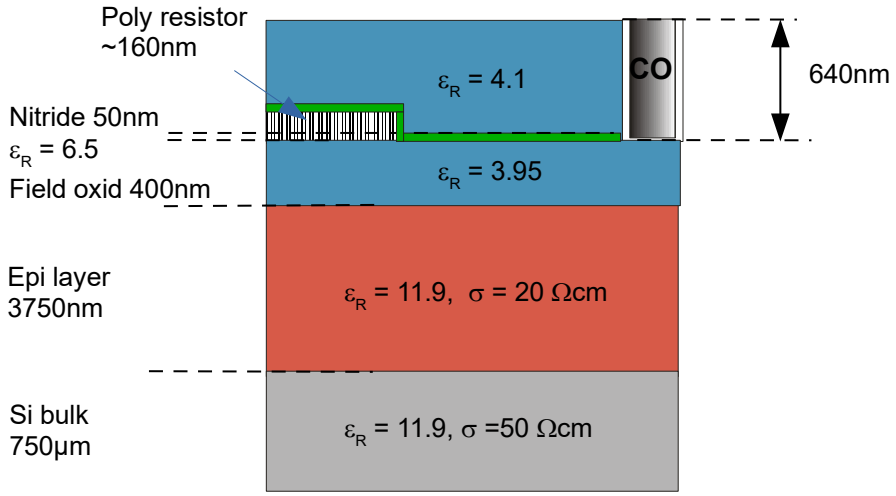


***Fig. 1.1.2:** BEOL detail cross-section below Metal1 for passive modeling (not to scale).*

Remark:
ILDO consists of oxide (590nm) and nitride (50nm).
For a homogenous ILDO with ε_R=4.1 the effective thickness corresponds to d_{eff}=620nm.

1.2 Process Control

Several geometrical and electrical parameters are measured for process control purposes. Electrical measurements are typically performed at T_0 = 27°C (300K). Coefficients describing the temperature behavior of parameters are extracted for the temperature range -40°C < T < 125°C.

Process control parameters are assigned to one of the following categories:

1.2.1 Pass/Fail Parameters

Pass/fail parameters are used for wafer selection during the wafer fabrication process. Pass/Fail parameters are measured on each wafer and are characterized by SPEC limits in **bold red.**

1.2.2 Information Parameters

Information parameters are provided in order to increase the knowledge about the process. These parameters do not lead to wafer scrap. There are two groups of information parameters:

The first group of information parameters is measured, identically to the pass/fail parameters, on each wafer. These parameters are characterized by SPEC limits in **bold blue.**

The second group of information parameters is not measured on each wafer. This group includes, for example, the layer thickness values measured during the wafer fabrication process or taken from REM cross-sections, and the coefficients describing the temperature, voltage and matching behavior of active and passive devices. This group of information parameters is given in *italic blue.*

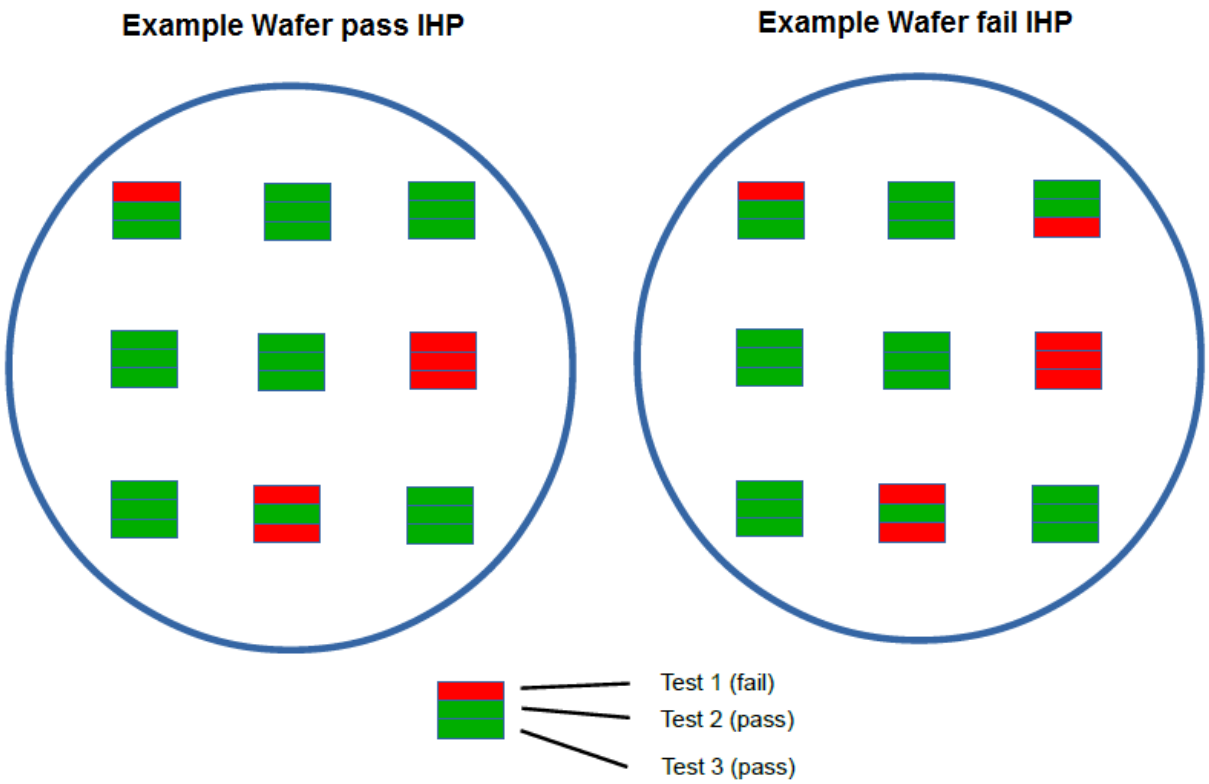
Notes:

- *The process control transistor parameters must not be used for circuit simulation purposes. They are often extracted from simplified model equations in order to increase the speed of the measurements. Special circuit simulation transistor parameters are provided in the model parameter section 5. Those are extracted from the complete set of model equations in order to give the best fit of the entire characteristic for all operating points. Therefore, process control transistor parameters may differ from their corresponding circuit simulation parameters.*
- *It is strongly recommended that a design shall rely only on pass/fail parameters.*

1.3 Wafer Reject Criteria

Pass/fail parameters are measured on nine (or more) sites, distributed uniformly across the wafer. At least 2/3 of the measured sites (min. 6 sites) must pass all pass/fail criteria in order to consider the tested wafer as pass.

Please refer to the following example. In reality about 50 tests are included.



2 Process Control Parameters

2.1 NMOS

$V_{GS} \leq 1{,}65$ V @ 125°C

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTN10x013	V	0.43	0.50	0.55	A.a1	WxL = 10 x 0.13 µm²
Threshold Voltage Long Channel Device	VTN10x10	V	0.16	0.20	0.24	A.a1	WxL = 10 x 10 µm²
Threshold Voltage Small Channel Device	VTN015x013	V	0.4	0.54	0.68	A.a1	WxL = 0.15 x 0.13 µm²
Saturation Current Short Channel Device	IDSN013	µA/µm	380	480	600	A.b1	WxL = 10 x 0.13 µm²
Off-Current Short Channel Device	IOFFN013	LOG10 (A/µm)		-10	-9	A.c1	WxL = 10 x 0.13 µm²
Drain Induced Barrier Lowering 0.1/1.2V	DIBLN013	mV/V	20	50	80	A.d1	WxL = 10 x 0.13 µm²
Sub Threshold Slope	SSN013	mV/dec	76	82	88	A.e	WxL = 10 x 0.13 µm²

Breakdown Voltage	BVDSSN013	V	**2.0**	**2.7**		A.f1	WxL = 10 x 0.13 µm²
Effective Channel Length	LEFFN013	µm	**0.10**	**0.14**	**0.19**	A.g1	WxL = 10 x 0.13 µm²
Effective Channel Width	WEFFN015	µm	**0.09**	**0.15**	**0.22**	A.h1	WxL = 0.15 x 0.13 µm²
Miller Capacitance NMOS	CMILLERN	fF/µm	**0.32**	**0.36**	**0.40**	A.k1	
Junction Capacitance NMOS	CJUNCTIONN	fF/µm²	**0.9**	**0.95**	**1.0**	A.k	
Junction Breakdown	BVNPW			*12*		A.f3	

2.2 PMOS

V_{GS} ≤ 1,65 V @ 125°C

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTP10x013	V	**-0.53**	**-0.47**	**-0.41**	A.a1	WxL = 10 x 0.13 µm²
Threshold Voltage Long Channel Device	VTP10x10	V	**-0.41**	**-0.36**	**-0.31**	A.a1	WxL = 10 x 10 µm²
Threshold Voltage Small Channel Device	VTP015x013	V	**-0.58**	**-0.48**	**-0.38**	A.a1	WxL = 0.15 x 0.13 µm²
Saturation Current Short Channel Device	IDSP013	µA/µm	**-270**	**-215**	**-170**	A.b1	WxL = 10 x 0.13 µm²
Off-Current Short Channel Device	IOFFP013	LOG10 (A/µm)		**-10.3**	**-9,3**	A.c1	WxL = 10 x 0.13 µm²
Drain Induced Barrier Lowering 0.1/1.2V	DIBLP013	mV/V	**25**	**50**	**75**	A.d1	WxL = 10 x 0.13 µm²
Sub Threshold Slope	SSP013	mV/dec	**-87**	**-81**	**-75**	A.e	WxL = 10 x 0.13 µm²
Breakdown Voltage	BVDSSP013	V		**-2.9**	**-2.2**	A.f1	WxL = 10 x 0.13 µm²
Effective Channel Length	LEFFP013	µm	**0.07**	**0.10**	**0.13**	A.g1	WxL = 10 x 0.13 µm²
Effective Channel Width	WEFFP015	µm	**0.17**	**0.24**	**0.31**	A.h1	WxL = 0.15 x 0.13 µm²
Miller Capacitance	CMILLERP	fF/µm	**0.31**	**0.35**	**0.39**	A.k1	
Junction Capacitance	CJUNCTIONP	fF/µm²	**0.8**	**0.85**	**0.9**	A.k	
Junction Breakdown	BVPNW	V		*-12*		A.f3	

2.3 iNMOS

V_{GS} ≤ 1,65 V @ 125°C

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTNI10x013	V	**0.43**	**0.50**	**0.55**	A.a1	WxL = 10 x 0.13 µm²
Saturation Current Short Channel Device	IDSNI013	µA/µm	**380**	**480**	**600**	A.b1	WxL = 10 x 0.13 µm²

Off-Current Short Channel Device	IOFFNI013	LOG10 (A/µm)		**-10**	**-9**	A.c1	WxL = 10 x 0.13 µm²
Drain Induced Barrier Lowering 0.1/1.2V	DIBLNI013	mV/V	**20**	**50**	**80**	A.d1	WxL = 10 x 0.13 µm²
Sub Threshold Slope	SSNI013	mV/dec	**76**	**82**	**88**	A.e	WxL = 10 x 0.13 µm²
Breakdown Voltage	BVDSSNI013	V	**2.0**	**2.7**		A.f1	WxL = 10 x 0.13 µm²

2.4 HV-NMOS

$V_{GS} \leq 3{,}3V$ (Maximum) @ 27°C for $L_G \geq 0{,}6$ µm

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTNHV10x045	V	**0.63**	**0.70**	**0.77**	A.a2	WxL = 10 x 0.45 µm²
Threshold Voltage Long Channel Device	VTNHV10x10	V	**0.65**	**0.69**	**0.73**	A.a2	WxL = 10 x 10 µm²
Threshold Voltage Small Channel Device	VTNHV030x045	V	**0.59**	**0.67**	**0.75**	A.a2	WxL = 0.30 x 0.45 µm²
Saturation Current Short Channel Device	IDSNHV045	µA/µm	**480**	**560**	**640**	A.b2	WxL = 10 x 0.45 µm²
Off-Current Short Channel Device	IOFFNHV045	LOG10 (A/µm)		**-12.5**	**-11.0**	A.c2	WxL = 10 x 0.45 µm²
Drain Induced Barrier Lowering 0.1/1.8V	DIBLNHV045	mV/V	**0**	**15**	**30**	A.d2	WxL = 10 x 0.45 µm²
Sub Threshold Slope	SSNHV045	mV/dec	**72**	**84**	**96**	A.e	WxL = 10 x 0.45 µm²
Breakdown Voltage	BVDSSNHV045	V	**5,3**	**6.1**		A.f2	WxL = 10 x 0.45 µm²
Effective Channel Length	LEFFNHV045	µm	**0.26**	**0.31**	**0.36**	A.g2	WxL = 10 x 0.45 µm²
Effective Channel Width	WEFFNHV030	µm	**0.23**	**0.28**	**0.33**	A.h2	WxL = 0.30 x 0.45 µm²
Miller Capacitance	CMILLERNHV	fF/µm	**0,42**	**0.45**	**0,48**	A.k1	
Junction Capacitance	CJUNC-TIONNHV	fF/µm²	**0,74**	**0,80**	**0,86**	A.k	
Junction Breakdown	BVNPWhv	V		*12*		A.f3	

2.5 HV-PMOS

$V_{GS} \leq 3{,}3V$ (Maximum) @ 27°C for $L_G \geq 0{,}5$ µm

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTPHV10x04	V	**-0.71**	**-0.65**	**-0.59**	A.a2	WxL = 10 x 0.4 µm²
Threshold Voltage Long Channel Device	VTPHV10x10	V	**-0.78**	**-0.70**	**-0.64**	A.a2	WxL = 10 x 10 µm²
Threshold Voltage Small Channel Device	VTPHV03x04	V	**-0.71**	**-0.64**	**-0.57**	A.a2	WxL = 0.3 x 0.4 µm²
Saturation Current Short Channel Device	IDSPHV04	µA/µm	**-290**	**-240**	**-190**	A.b2	WxL = 10 x 0.4 µm²
Off-Current Short Channel Device	IOFFPHV04	LOG10 (A/µm)		**-12.5**	**-11.5**	A.c2	WxL = 10 x 0.4 µm²

Drain Induced Barrier Lowering 0.1/3.3V	DIBLPHV04	mV/V	**0**	**5**	**15**	A.d2	WxL = 10 x 0.4 µm²
Sub Threshold Slope	SSPHV04	mV/dec	**-102**	**-92**	**-82**	A.e	WxL = 10 x 0.4 µm²
Breakdown Voltage	BVDSSPHV04	V		**-6.3**	**-5.3**	A.f2	WxL = 10 x 0.4 µm²
Effective Channel Length	LEFFPHV04	µm	**0.24**	**0.30**	**0.36**	A.g2	WxL = 10 x 0.4 µm²
Effective Channel Width	WEFFPHV03	µm	**0.26**	**0.33**	**0.40**	A.h2	WxL = 0.3 x 0.4 µm²
Miller Capacitance	CMILLERPHV	fF/µm	**0.32**	**0.35**	**0.38**	A.k1	
Junction Capacitance	CJUNCTION-PHV	fF/µm²	**0.74**	**0.80**	**0.86**	A.k	
Junction Breakdown	BVPNWhv	V		*-12*		A.f3	

2.6 HV-iNMOS

$V_{GS} \leq$ 3,3V (Maximum) @ 27°C for $L_G \geq$ 0,6 µm

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Threshold Voltage Short Channel Device	VTNIHV10x045	V	**0.63**	**0.70**	**0.77**	A.a2	WxL = 10 x 0.45 µm²
Saturation Current Short Channel Device	IDSNIHV045	µA/µm	**480**	**560**	**640**	A.b2	WxL = 10 x 0.45 µm²
Off-Current Short Channel Device	IOFFNIHV045	LOG10 (A/µm)		**-12.5**	**-11.0**	A.c2	WxL = 10 x 0.45 µm²
Drain Induced Barrier Lowering 0.1/1.8V	DIBLNIHV045	mV/V	**0**	**15**	**30**	A.d2	WxL = 10 x 0.45 µm²
Sub Threshold Slope	SSNIHV045	mV/dec	**72**	**84**	**96**	A.e	WxL = 10 x 0.45 µm²
Breakdown Voltage	BVDSSNIHV045	V	**5.2**	**6.1**		A.f2	WxL = 10 x 0.45 µm²

2.7 Rsil

Rsil utilizes ***salicided, n-doped gate polysilicon*** as resistor material

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Sheet Resistance	RSNRSIL	Ω	**6.2**	**7.0**	**7.8**	A.i	
Line Width Delta	DWRSIL	nm	**-20**	**10**	**40**	A.i	
Temperature Coefficients	TC1NRSIL TC2NRSIL	ppm/K ppm/K²		*3100* *0.3*		A.af	
Matching Coefficient	MATRSIL1 MATRSIL2	nm		*6* *1.4*		A.ac	
Metal-to-Body-Resis-tance	RCRSIL			*4.5*		A.ae	
Max. Current Density	is limited by contacts, please refer chapter 2.9						

2.8 Rppd

Rppd utilizes ***unsalicided, p-doped gate polysilicon*** as resistor material. For realizing precision resistors, a line width of 2µm or higher is recommended.

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Sheet Resistance	RSRPPD	Ω	**235**	**260**	**285**	A.i	
Line Width Delta	DWRPPD	nm	**-24**	**6**	**36**	A.i	
Temperature Coefficients	TC1NRPPD TC2NRPPD	ppm/K ppm/K^2		*170* *0.4*		A.af	
Matching Coefficient	MATRPPD	nm		*15*		A.ac	
Metal-to-Body-Resistance	RCRPPD	Ω*µm		*35*		A.ae	
Temperature Coefficient Metal-toBody-Resistance	TC3NRPPD	ppm/K		*-950*			
Max. Current Density	IMRPPD	mA/µm			*1.2*		11 years @105°C

2.9 Rhigh

Rhigh utilizes ***unsalicided, partially compensated gate polysilicon*** as resistor material

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Sheet Resistance	RSRHIGH	Ω	**1160**	**1360**	**1560**	A.i	
Line Width Delta	DWRHIGH	nm	**-80**	**-40**	**0**	A.i	
Temperature Coefficients	TC1NRHIGH TC2NRHIGH	ppm/K ppm/K²		*-2300* *2.1*		A.af	
Matching Coefficient	MATRHIGH	nm		*48*		A.ac	
Metal-to-Body-Resis-tance	RCRHIGH	Ω*µm		*80*		A.ae	
Max. Current Density	IMRHIGH	mA/µm			*0.6*		11 years @105°C

2.10 Schottky_nbl1

This Schottky barrier diode utilizes ***Nbulay*** as cathode.

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Reverse current density	IRNBL1	µA/µm²	**-1**	**-0.1**	**0**		0.3 x 1.0 µm² @ -2.5 V
Diode Voltage	VFNBL1	V	**0.34**	**0.39**	**0.44**		0.3 x 1.0 µm² @ 100 µA/µm²

2.11 S-Varicap

Thick Gate Oxide

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Capacitance -3	SVAR_m3	fF/µm²	**20.5**	**23**	**25.5**		10x(3.74x0.3)µm² @15.8GHz
Capacitance 0	SCVAR_0	fF/µm²	**32**	**35.3**	**37.5**		10x(3.74x0.3)µm² @15.8GHz
Capacitance +3	SCVAR_3	fF/µm²	**37.5**	**39.5**	**41.5**		10x(3.74x0.3)µm² @15.8GHz
Q Factor -3	QFACTOR_m3		**50**	**62**	**75**		10x(3.74x0.3)µm² @15.8GHz
Q Factor 0	QFACTOR_0		**35**	**43**	**50**		10x(3.74x0.3)µm² @15.8GHz
Q Factor 3	QFACTOR_3		**35**	**43**	**50**		10x(3.74x0.3)µm² @15.8GHz

2.12 MIM Capacitor

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Specific Area Capacitance	CMIMA	fF/µm²	**1.35**	**1.5**	**1.65**	A.k	
Specific Capacitance MIM Perimeter	CMIMP	aF/µm		*40*		A.l	
Breakdown Voltage	BVMIM	V	**15**	**23**		A.y	
Voltage Coefficients	VCMIM1 VCMIM2	ppm/V ppm/V²		*-26* *5*		A.ah	
Temperature Coefficient	TCMIM1 TCMIM2	ppm/K ppm/K²		*3.6* *0.002*		A.ad	
Matching Coefficient	KCMIM	nm					

2.13 Resistances, Line Width Deltas, Temperature Coefficients

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Substrate Resistivity	RSBLK	Ωcm	*37.5*	*50*	*62.5*		Specification: WAFPR3763
Salicided GatPoly (n^+)	refer section 2.13						
Unsalicized GatPoly (n^+)	refer section 2.14						
Unsalicided GatPoly (p^+)	refer section 2.15						
Metal1 Snake Sheet Resistance	SNAKEM1	mΩ	90	115	145		width = 0.16 µm
Unsalicided nSD-Activ Sheet Resistance	RSNSD0	Ω	55	67	79		
Unsalicided pSD-Activ Sheet Resistance	RSPSD0	Ω	69	79	89		
Metal2 Snake Sheet Resistance	SNAKEM2	mΩ	70	88	110		width = 0.20 µm
Metal3 Snake Sheet Resistance	SNAKEM3	mΩ	70	88	110		width = 0.20 µm
Metal4 Snake Sheet Resistance	SNAKEM4	mΩ	70	88	110		width = 0.20 µm
Metal5 Snake Sheet Resistance	SNAKEM5	mΩ	70	88	110		width = 0.20 µm
TopMetal1 Snake Sheet Resistance	SNAKETM1	mΩ	14	18	22		width = 1.5 µm
TopMetal2 Snake Sheet Resistance	SNAKETM2	mΩ	7.5	11	14.5		width = 2.0 µm
Metal1 Sheet Resistance	RSMET1	mΩ	85	110	135	A.i	
Metal2 Sheet Resistance	RSMET2	mΩ	73	88	103	A.i	
Metal3 Sheet Resistance	RSMET3	mΩ	73	88	103	A.i	
Metal4 Sheet Resistance	RSMET4	mΩ	73	88	103	A.i	
Metal5 Sheet Resistance	RSMET5	mΩ	73	88	103	A.i	
TopMetal1 Sheet Resistance	RSTM1	mΩ	15	18	21	A.i	
TopMetal2 Sheet Resistance	RSTM2	mΩ	7.5	11	14.5	A.i	
Metal1 Line Width Delta	DWMET1	nm	-64	-24	16	A.i	
Metal2 Line Width Delta	DWMET2	nm	-56	-16	24	A.i	
Metal3 Line Width Delta	DWMET3	nm	-56	-16	24	A.i	
Metal4 Line Width Delta	DWMET4	nm	-56	-16	24	A.i	
Metal5 Line Width Delta	DWMET5	nm	-50	-20	34	A.i	
TopMetal1 Line Width Delta	DWTM1	nm	-300	-100	100	A.i	
TopMetal2 Line Width Delta	DWTM2	nm	-340	-140	140	A.i	
Metal1 Sheet Resistance Temperature Coefficient	TC1RSMET1	ppm/K		*3400*		A.af	
Metal2 Sheet Resistance	TC1RSMET2	ppm/K		*3500*		A.af	

Temperature Coefficient							
Metal3 Sheet Resistance Temperature Coefficient	TC1RSMET3	ppm/K		*3500*		A.af	
Metal4 Sheet Resistance Temperature Coefficient	TC1RSMET4	ppm/K		*3500*		A.af	
Metal5 Sheet Resistance Temperature Coefficient	TC1RSMET5	ppm/K		*3500*		A.af	
TopMetal1 Sheet Resistance Temperature Coefficient	TC1RSTM1	ppm/K		*3700*		A.af	
TopMetal2 Sheet Resistance Temperature Coefficient	TC1RSTM2	ppm/K		*3800*		A.af	

2.14 Contact & Via Resistances

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Metal1 to Silicide on nSD-Activ	RCM1NSD	Ω/CNT	**8**	**17**	**22**	V = 1 V	93740 contact chain
Metal1 to Silicide on pSD-Activ	RCM1PSD	Ω/CNT	**8**	**17**	**22**	V = 1 V	93740 contact chain
Metal1 to Silicide on GatPoly (n^+)	RCM1NPLY	Ω/CNT	**8**	**15**	**20**	V = 1 V	98566 contact chain
Metal1 to Silicide on GatPoly (p^+)	RCM1PPLY	Ω/CNT	**8**	**15**	**20**	V = 1 V	98566 contact chain
Metal2 – Metal1	RVIA1	Ω/VIA	**5**	**9**	**20**	V = 1 V	103840 contact chain
Metal3 – Metal2	RVIA2	Ω/VIA	**5**	**9**	**20**	V = 1 V	103840 contact chain
Metal4 – Metal3	RVIA3	Ω/VIA	**5**	**9**	**20**	V = 1 V	103840 contact chain
Metal5 – Metal4	RVIA4	Ω/VIA	**5**	**9**	**20**	V = 1 V	103840 contact chain
TopMetal1 – Metal5	RTV1	Ω/VIA	**1**	**2.2**	**4**	V = 1 V	3276 contact chain
TopMetal2 – TopMetal1	RTV2	Ω/VIA	**0.5**	**1.1**	**2.2**	V = 1 V	1140 contact chain

2.15 Maximum Current Densities

(11 years @105°C)

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Metal1	IMAXM1	mA			*0.36*	A.v	w = 0.16 ... 0.36 µm
Metal1	JMAXM1	mA/µm			*1*	A.v	w > 0.36 µm
Metal2	IMAXM2	mA			*0.6*	A.v	w = 0.2 … 0.3 µm
Metal2	JMAXM2	mA/µm			*2*	A.v	w > 0.3 µm
Metal3	IMAXM3	mA			*0.6*	A.v	w = 0.2 … 0.3 µm
Metal3	JMAXM3	mA/µm			*2*	A.v	w > 0.3 µm
Metal4	IMAXM4	mA			*0.6*	A.v	w = 0.2 … 0.3 µm
Metal4	JMAXM4	mA/µm			*2*	A.v	w > 0.3 µm
Metal5	IMAXM5	mA			*0.6*	A.v	w = 0.2 … 0.3 µm
Metal5	JMAXM5	mA/µm			*2*	A.v	w > 0.3 µm
TopMetal1	JMAXM6	mA/µm			*15*	A.v	
TopMetal2	JMAXM7	mA/µm			*16*	A.v	
Contact	JMAXCNT	mA/Cnt			*0.3*	A.v	
Via1	JMAXVIA1	mA/Via			*0.4*	A.v	
Via2	JMAXVIA2	mA/Via			*0.4*	A.v	
Via3	JMAXVIA3	mA/Via			*0.4*	A.v	
Via4	JMAXVIA4	mA/Via			*0.4*	A.v	
TopVia1	JMAXTVIA1	mA/Via			*1.4*	A.v	
TopVia2	JMAXTVIA2	mA/Via			*10*	A.v	

2.16 Layer Thickness Values

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Shallow Trench Isolator Thickness	TSTI	nm		400		A.ag	
Gate Polysilicon Thickness	TGATPOLY	nm	150	160	170	A.w	
Thickness of Gate Oxide	TGOXNW	nm	2.25	2.45	2.65	A.x	
Thickness of Gate Oxide HV-MOS	TGOX1NW	nm	6.8	7.3	7.8	A.x	
Thickness of Gate Oxide	TGOXPW	nm	2.45	2.65	2.85	A.x	
Thickness of Gate Oxide HV-MOS	TGOX1PW	nm	7.0	7.5	8.0	A.x	
Metal1 Layer Thickness	TMET1	nm		420		A.ag	
Metal2 Layer Thickness	TMET2	nm		490		A.ag	
Metal3 Layer Thickness	TMET3	nm		490		A.ag	
Metal4 Layer Thickness	TMET4	nm		490		A.ag	
Metal5 Layer Thickness	TMET5	nm		490		A.ag	
TopMetal1 Layer Thickness	TTM1	nm		2000		A.ag	
Isolator Thickness between Metal1 and Activ	TILD0	nm		640		A.w, A.ag	
Isolator Thickness between Metal2 and Metal1	TILD1	nm		540		A.w, A.ag	
Isolator Thickness between Metal3 and Metal2	TILD2	nm		540		A.w, A.ag	
Isolator Thickness between Metal4 and Metal3	TILD3	nm		540		A.w, A.ag	
Isolator Thickness between Metal5 and Metal4	TILD4	nm		540		A.w, A.ag	
Isolator Thickness between TopMetal1 and Metal5	TILDTM1	nm		850		A.w, A.ag	
MIM Capacitor Dielectric Thickness	TISMIM	nm		40		A.w	
MIM Capacitor Top Plate Thickness	TMIMTOP	nm		150		A.ag	
Thickness Values of Passivation Layers	TPASS1 TPASS2	nm		1500 400		A.ag	Oxide layer SiN layer
TopMetal2 Layer Thickness	TTM2	nm		3000		A.ag	
Isolator Thickness between TopMetal2 and TopMetal1	TILTM2	nm		2800		A.w, A.ag	

2.17 Parasitic Capacitances

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Metal1 - Activ Area Capacitance	CAMET1ACT	aF/µm²	**49**	**59**	**69**	A.aq	A = 250·1200 µm²
Metal1 - Substrate Area Capacitance	CAMET1SUB	aF/µm²	**31**	**37**	**43**	A.aq	A = 250·1200 µm²
Metal1 - Metal2 Area Capacitance	CAMET1/2	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
Metal2 - Metal3 Area Capacitance	CAMET2/3	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
Metal3 - Metal4 Area Capacitance	CAMET3/4	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
Metal4 - Metal5 Area Capacitance	CAMET4/5	aF/µm²	**54**	**68**	**82**	A.aq	A = 250·1200 µm²
TopMetal1 - Metal5 Area Capacitance	CATOPMET1	aF/µm²	**36**	**42.5**	**49**	A.aq	A = 250·1200 µm²
TopMetal2 - TopMetal1 Area Capacitance	CATOPMET2	aF/µm²	**10**	**13**	**16**	A.aq	A = 250·1200 µm²

3 Bipolar Parameters

Important Note: *For process control monitoring minimum devices are used.*

3.1 npn13g2

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Current Gain	NPN13G2_BETA	-	**300**	**650**	**1200**	A.n	A_E=0.07x0.9 µm²
Early Voltage	NPN13G2_VA	V		*150*		A.o	A_E=0.07x0.9 µm²
Breakdown Voltage Emitter – Collector	NPN13G2_BVCEO	V	**1.4**	**1.6**		A.p	A_E=0.07x0.9 µm²
Breakdown Voltage Collector – Base	NPN13G2_BVCBO	V	**3.8**	**4.8**		A.q	A_E=0.07x0.9 µm²
Breakdown Voltage Emitter – Base	NPN13G2_BVEBO	V	**1.0**	**1.6**		A.r	A_E=0.07x0.9 µm²
Collector Current	NPN13G2_IC07	µA	**2.6**	**3.8**	**5.2**	A.ai	A_E=0.07x0.9 µm²
Max. Collector Cur-rent	NPN13G2_ICMAX	mA			*3.5*		A_E=0.07x0.9 µm²
Max. Transit Frequency	NPN13G2_FT	GHz	**300**	**350**		A.s	A_E=4x(0.07x0.9 µm²)
Max. Oszillation Frequency	NPN13G2_FMAX	GHz	**400**	**450**		A.s	A_E=4x(0.07x0.9 µm²)

3.2 npn13g2l

Parameter	Name	Unit	Min	Tar-get	Max	Meas. Cond.	Comment
Current Gain	NPN13G2L_BETA	-	**300**	**650**	**1200**	A.n	A_E=0.07x1 µm²
Early Voltage	NPN13G2L_VA	V		*150*		A.o	A_E=0.07x1 µm²
Breakdown Voltage Emitter – Collector	NPN13G2L_BVCEO	V	**1.4**	**1.6**		A.p	A_E=0.07x1 µm²
Breakdown Voltage Collector – Base	NPN13G2L_BVCBO	V	**3.8**	**4.8**		A.q	A_E=0.07x1 µm²
Breakdown Voltage Emitter – Base	NPN13G2L_BVEBO	V	**1.0**	**1.6**		A.r	A_E=0.07x2 µm²
Collector Current	NPN13G2L_IC07	µA	**2.6**	**3.8**	**5.2**	A.ai	A_E=0.07x1 µm²
Max. Collector Cur-rent	NPN13G2L_ICMAX	mA			*3.0*		A_E=0.07x1 µm²
Max. Transit Frequency	NPN13G2L_FT	GHz	**280**	**330**		A.s	A_E=4x(0.07x1 µm²)
Max. Oszillation Frequency	NPN13G2L_FMAX	GHz	**380**	**430**		A.s	

3.3 npn13g2v

Parameter	Name	Unit	Min	Target	Max	Meas. Cond.	Comment
Current Gain	NPN13G2V_BETA	-	**300**	**650**	**1200**	A.n	A_E=0.12x1 µm²
Early Voltage	NPN13G2V_VA	V		*150*		A.o	A_E=0.12x1 µm²
Breakdown Voltage Emitter – Collector	NPN13G2V_BVCEO	V	**2.2**	**2.5**		A.p	A_E=0.12x1 µm²
Breakdown Voltage Collector – Base	NPN13G2V_BVCBO	V	**7**	**8.5**		A.q	A_E=0.12x1 µm²
Breakdown Voltage Emitter – Base	NPN13G2V_BVEBO	V	**1.0**	**1.8**		A.r	A_E=0.12x1 µm²
Collector Current	NPN13G2V_IC07	µA	**3.4**	**4.7**	**6.2**	A.ai	A_E=0.12x1 µm²
Max. Collector Current	NPN13G2V_ICMAX	mA			*0.5*		A_E=0.12x1 µm²
Max. Transit Frequency	NPN13G2V_FT	GHz	**90**	**120**		A.s	A_E=4x(0.12x1 µm²)
Max. Oszillation Frequency	NPN13G2V_FMAX	GHz	**280**	**330**		A.s	

4 Attachment A: Measurement Conditions

Ref.	Parameter:
A.a1	**Threshold Voltage:** V_{DS} = +0.05 V / -0.05 V (n-channel / p-channel device); V_{BS} = 0 V; V_T is extrapolated from the maximum slope of the active transfer characteristic region. A linear regression is performed to find this slope. V_T = Vo – V_{DS}/2; Vo is the gate voltage intercept of the slope. Isolated NMOS: V_{nWell} = 0 V
A.a2	**Threshold Voltage:** V_{DS} = +0.1 V / -0.1 V (n-channel / p-channel device); V_{BS} = 0V; V_T is extrapolated from the maximum slope of the active transfer characteristic region. A linear regression is performed to find this slope. V_T = Vo – V_{DS}/2; Vo is the gate voltage intercept of the slope. Isolated NMOS: V_{nWell} = 0 V
A.b1	**Saturation Current:** V_{DS} = V_{GS}= +1.2 V / -1.2 V (n-channel / p-channel device); V_{BS} = 0 V Isolated NMOS: V_{nWell} = 0 V
A.b2	**Saturation Current:** V_{DS} = V_{GS}= +3.3 V / -3.3 V (n-channel / p-channel device); V_{BS} = 0 V Isolated NMOS: V_{nWell} = 0 V
A.c1	**Off-Current:** V_{DS}=+1.2V / -1.2V (n-channel device / p-channel device); V_{GS}=V_{BS}=0 V; I_D measured
A.c2	**Off-Current:** V_{DS}=+3.3V / -3.3V (n-channel device / p-channel device); V_{GS}=V_{BS}=0 V; I_D measured
A.d1	**Drain Induced Barrier Lowering:** DIBL = [V_{GS}(V_{DS1}) – V_{GS}(V_{DS2})]/(V_{DS1}-V_{DS2}) at I_D = JSS*W/L V_{DS1} = +0.1 V; V_{DS2} = +1.2 V; V_{BS} = 0 V; JSS = 0.5 nA (n-channel device) V_{DS1} = -0.1 V; V_{DS2} = -1.2 V; V_{BS}= 0 V; JSS = 0.1 nA (p-channel device)
A.d2	**Drain Induced Barrier Lowering:** DIBL = [V_{GS}(V_{DS1}) – V_{GS}(V_{DS2})]/(V_{DS1}-V_{DS2}) at I_D = ISS*W/L V_{DS1} = +0.1 V; V_{DS2} = +3.3 V; V_{BS} = 0 V; ISS = 1 nA (n-channel device) V_{DS1} = -0.1 V; V_{DS2} = -3.3 V; V_{BS}= 0 V; ISS = 0.4 nA (p-channel device)
A.e	**Sub Threshold Slope:** V_{DS} = +0.1 V / -0.1 V (n-channel / p-channel device); V_{BS} = 0 V The slope is estimated from the two drain currents I_{D1} = JSS1*W/L and I_{D2} = JSS2*W/L JSS1 = 0.5 nA, ISS2 = 5 nA (n-channel device); JSS1 = 0.1 nA, ISS2 = 1 nA (p-channel device);
A.f1	**Breakdown Voltage:** V_{GS}=V_{BS}=0 V; I_D=I_{Do}=+10 nA/µm / -10 nA/µm (n-channel / p-channel device)
A.f2	**Breakdown Voltage:** V_{GS} = V_{BS} = 0V; I_D = +100 pA/µm / -100 pA/µm (n-channel / p-channel device)
A.f3	**Breakdown Voltage:** j = 1 mA / cm² for S/D to body diode surrounded by STI
A.g1	**Effective Channel Length:** Extrapolated from linear regions of transistors with gate length's of 0.13 µm, 0.18 µm; V_{DS}=+0.05 V / -0.05 V (n-channel / p-channel device) Method (P. Suciu et.al., e.g. IEEE Tr. ED-27(1980)9,p.1846): Basic equations: (1) I_D = ✓ (V_{GSeff} – V_{DS}/2) V_{DS} (2) V_{GSeff} = V_{GS}– V_t (3) µ = $µ_o$ / (1 + U_o V_{GSeff}) (4) 1/✓(V_{GSeff}) = (L – ↯L) / (W µ C_{ox}) = (L – ↯L) (1 + U_o V_{GSeff}) / (W $µ_o$ C_{ox}) (5) 1/✓$_o$(L) = (L - ↯L) / (W $µ_o$ C_{ox}) First step: according to equ.(4), linear extrapolation of 1/✓$_o$ = 1/✓(V_{GSeff} = 0) from two working points V_{GSeff1} = +0.9V / -0.9V; V_{GSeff2} = +1.5V / -1.5V (n-channel / p-channel device) for all transistors with different gate length Second step: linear regression of ↯L from all 1/✓$_o$(L) numbers according to equ.(5)
A.g2	**Effective Channel Length:** Extrapolated from linear regions of transistors with gate length's of 0.33 µm (only SG13S), 0.45 µm, 10 µm / 0.33 µm (only SG13S) 0,4 µm, 10 µm; V_{DS}=+0.1 V / -0.1 V (n-channel / p-channel device) Method (P. Suciu et.al., e.g. IEEE Tr. ED-27(1980)9,p.1846): Basic equations: (1) I_D = β (V_{GSeff} – V_{DS}/2) V_{DS}

(2) $V_{GSeff} = V_{GS} - V_t$
(3) $\mu = \mu_o / (1 + U_o V_{GSeff})$
(4) $1/\beta(V_{GSeff}) = (L - \Delta L) / (W \mu C_{ox}) = (L - \Delta L) (1 + U_o V_{GSeff}) / (W \mu_o C_{ox})$
(5) $1/\beta_o(L) = (L - \Delta L) / (W \mu_o C_{ox})$
First step: according to equ.(4), linear extrapolation of $1/\beta_o = 1/\beta(V_{GSeff} = 0)$ from two working points V_{GSeff1} = +1V / -1V; V_{GSeff2} = +1.5V / -1.5V (n-channel / p-channel device) for all transistors with different gate length
Second step: linear regression of ΔL from all $1/\beta_o(L)$ numbers according to equ.(5)

A.h1 **Effective Channel Width:**
Extrapolated from linear regions of transistors with gate width's of 0.15µm, 10.0 µm (not isolated NMOS), V_{DS} = +0.05 V / -0.05 V (n-channel / p-channel device)
Basic equations:
(1) $I_D = \beta (V_{GSeff} - V_{DS}/2) V_{DS}$
(2) $V_{GSeff} = V_{GS} - V_T$
(3) $\mu = \mu_o / (1 + U_o V_{GSeff})$
1. $1/\beta(V_{GSeff}) = L / [(W - \Delta W) \mu C_{ox}] = [L (1 + U_o V_{GSeff})] / [(W - \Delta W) \mu_o C_{ox}]$
2. $\beta_o(W) = (W - \Delta W) \mu_o C_{ox} / L$

First step: according to equ.(4), linear extrapolation of $1/\beta_o = 1/\beta(V_{GSeff} = 0)$ from two working points V_{GSeff1} = +1V / -1V; V_{GSeff2} = +1.5V / -1.5V (n-channel / p-channel device) for all transistors with different gate width
Second step: linear regression of ΔW from all $\beta_o(W)$ numbers according to equ.(5)

A.h2 **Effective Channel Width:**
Extrapolated from linear regions of transistors with gate width's of 0.3 µm, 10.0 µm ,
V_{DS} = +0.1 V / -0.1 V (n-channel / p-channel device)
Basic equations:
(1) $I_D = \beta (V_{GSeff} - V_{DS}/2) V_{DS}$
(2) $V_{GSeff} = V_{GS} - V_T$
(3) $\mu = \mu_o / (1 + U_o V_{GSeff})$
3. $1/\beta(V_{GSeff}) = L / [(W - \Delta W) \mu C_{ox}] = [L (1 + U_o V_{GSeff})] / [(W - \Delta W) \mu_o C_{ox}]$
4. $\beta_o(W) = (W - \Delta W) \mu_o C_{ox} / L$

First step: according to equ.(4), linear extrapolation of $1/\beta_o = 1/\beta(V_{GSeff} = 0)$ from two working points V_{GSeff1} = +1V / -1V; V_{GSeff2} = +1.5V / -1.5V (n-channel / p-channel device) for all transistors with different gate width
Second step: linear regression of ΔW from all $\beta_o(W)$ numbers according to equ.(5)

A.i **Sheet Resistance, Line Width Delta**
The sheet resistance R_s and the line width delta (= ΔW) values are calculated from the resistances of two resistors R_1 and R_N:
- R_1: one single stripe with the dimension W x L
- R_N: N stripes in parallel with dimensions (W/N) x L each

Formulas: $R_1 = R_s L / (W + \Delta W)$ and $R_N = R_s (L / N) / (W/N + \Delta W)$
Voltage across both resistors in series: 0.5V

A.k **Capacitance Measurements, Area Capacitances**
V=0V; f=100kHz; Area Capacitance = $C_{measure}$ / Area

A.k1 **Capacitance Measurements MIM, Area Capacitances**
V=2V applied to top plate; f=100kHz

A.l **Capacitance Measurements, Perimeter Capacitance**
V=0V; f=100kHz
Perimeter capacitance = [$C_{measure}$ / Perimeter

A.n **Current Gain**
BETA = I_C / I_B; V_{BE}=0.7V; V_{CB}=0V

A.o **Early Voltage**
VCE = 0.9 ± 0.2 V; IB = const = IB(VBE = 0.70 V; VCB = 0 V)

A.p **Breakdown Voltage BV_{CE0}**
Extrapolation from the J_C=(0.3 – 0.75)mA/µm² part of the $V_{CE}(I_C)$ characteristic, J_C related to the emitter area A_E

A.q **Breakdown Voltage BV_{CB0}**
I_E=0; I_{CB}=0.1µA

A.r **Breakdown Voltage BV_{EB0}**
I_C=0; I_{EB}=1µA

A.s **HBT Maximum Transit Frequency (f_T), HBT Maximum Oscillation Frequency (f_{max})**
U and h_{21} are measured as a function of V_{BE} @ V_{CE} = 1.2 V and 40 GHz. f_T and f_{max} are extrapolated, with -

20dB decay per f-decade, from the 40 GHz h_{21} and sqrt(U) values, respectively. De-embedding is applied.

A.v **Maximum Current Density of Metal Lines, Contacts and Vias**
The maximum current density is determined via electromigration measurements as part of the process qualification procedure. The current density values given were estimated to reach less than 0.01% failure in 11years of operation at 105°C (for SG13RH: 20 years at 125°C)

A.x **Gateoxide thickness measurement using Cox extrapolation**
Measured capacitance corrected for Offset and Miller Capacitance. Tox = 3.9*Eps0*Area/Cox

A.w **Optical Layer Thickness**
The thickness of the layer is measured by means of optical interferometry / ellipsometry

A.y **MIM Breakdown Voltage**
V_{BOTTOM}=0V; J_{BVMIM}=1 pA/µm²
BV_{MIM} : Current forced into the top plate and corresponding voltage is measured.

A.ac **Resistor Matching Coefficient k**
Measuring the matching behavior of resistor pairs, differing in the resistor area, are investigated. The least square fit σ(dR/R) vs. inverse square root of area is estimated: $\sigma(dR/R) = k*A^{-0.5}$

A.ad **MIM Capacitor Temperature Coefficient**
Measurement of capacitance (at V_{MIM} = 0V, f = 1MHz) as a function of temperature in the range -40°C to 125°C.
Temperature coefficients T_{CMIM1} and T_{CMIM2}; T_0 = 300K
$C(T) = C(T_0) * [1 + T_{CMIM1} * (T - T_0) + T_{CMIM2} * (T - T_0)^2]$

A.ae **Salicide to GatPoly Contact Resistance**
$R_{RES} = (2* R_{CONT} / \#\text{ of contacts}) + (2* R_{C2POLY} / \text{resistor width}) + R_{POLY}$
Note that this formula is only valid for resistors with same width of unsalicided and salicided regions
R_{RES}: Total resistance of a resistor; R_{CONT}: Contribution of a single W-plug (typically < 1Ω)
R_{C2POLY}: Salicide to GatPoly contact resistance
R_{POLY}: Contribution of the unsalicided polysilicon stripe (= R_S* L / W)

A.af **Resistor Temperature Coefficients**
Measurement of R as a function of temperature in the range -40°C to 125°C.
Temperature coefficients T_{C1} and T_{C2}; T_0 = 300K
$R(T) = R(T_0) * [1 + T_{C1} * (T - T_0) + T_{C2} * (T - T_0)^2]$

A.ag **SEM Cross Section Analysis**

A.ah **MIM Capacitor Voltage Coefficients**
Measurement of capacitance (at T = 300K, f = 1MHz) as a function of the applied voltage (V_{MIM}) in the range -10V to +10V. V_{MIM} is applied at the lower electrode, while the top electrode is grounded.
$C(V_{MIM}) = C(V_{MIM}=0V) * [1 + VCMIM1 * (V_{MIM}) + VCMIM2 * (V_{MIM})^2]$

A.ai **Collector Current**
V_{BE}=0.7V; V_{CB}=0V

A.al **HBT Transistor Matching Coefficient k**
Measuring the matching behavior of transistor pairs, differing in the emitter area, are investigated. The least square fit σ(dVBE) vs. inverse square root of area is estimated: $\sigma(dVBE) = k*A^{-0.5}$
V_{BE}=0.7V; V_{CB}=0V

A.am **MOS Transistor Matching Coefficient k**
Measuring transistor pairs, differing in the gate area. The least square fit σ(dVT) vs. inverse square root of area is estimated: $\sigma(dVT) = k*A^{-0.5}$
V_{DS}=0.1 V; I_D=2µA W/L

A.aq **Capacitance of metal layer to Active or Substrate**
V=0V; f=100kHz

5 Change History

Version	Changes/Remarks
2023_02_21 1.0	Initial Version
2023_03_27 1.1	License text added, minor document updates
2023_12_20 1.2	Section 2 Updated Information for MOS Devices

6 Known Issues